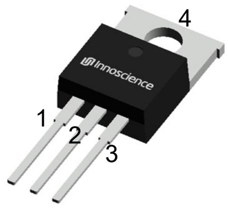
INN700TH240B

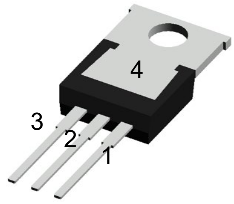
1. General description

700V GaN-on-Silicon Enhancement-mode Power Transistor in TO-220 package.

2. Features

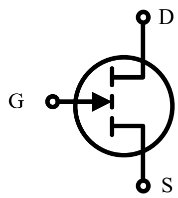
- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant





3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	240	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	2	nC
$I_{D,pulse}$	18	A
Q_{OSS} @ V_{DS} = 400 V	21	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Source	Drain
1	2,4	3

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN700TH240B	TO-220	70TH240B

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,\ max}$	700	V	V_{GS} = 0 V; T_j = -55 °C to 150 °C
Drain source voltage transient [1]	$V_{DS,\ transient}$	800	V	V_{GS} = 0 V
Drain source voltage, pulsed [2]	$V_{DS,\ pulse}$	750	V	T_j = 25 °C; total time < 10 h T_j = 125 °C; total time < 1 h
Continuous current, drain source	I_D	10	A	T_c = 25 °C
Pulsed current, drain source [3]	$I_{D,\ pulse}$	18	A	T_c = 25 °C; V_{GS} = 6 V; t_{PULSE} = 10 μs
Pulsed current, drain source [3]	$I_{D,\ pulse}$	10	A	T_c = 125 °C; V_{GS} = 6 V; t_{PULSE} = 10 μs
Gate source voltage, continuous [4]	V_{GS}	-1.4 to +7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,\ pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	63	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1. $V_{DS,\ transient}$ is intended for non-repetitive events, t_{PULSE} < 200 μs.

2. $V_{DS,\ pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns.

3. Limit was extracted from characterization test, not measured during production.

4. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10.

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA} [1]	43	°C/W	
Thermal resistance, junction-case (bottom)	R_{thJC_bot}	1.96	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	

1.R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D = 11 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.7	-		I_D = 11 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.4	20	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	5	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	50	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	165	240	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 25 °C
		-	360	-	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 150 °C
Gate resistance	R_G	-	6	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	79	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	25	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.2	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	36	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	52	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	21	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	V_{DS} = 400 V; I_D = 6 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω; See Figure 22
Turn-off delay time	$t_{d(off)}$	-	4	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	6	-	ns	

1. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.

2. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 3 A
Gate-source charge	Q_{GS}	-	0.2	-	nC	
Gate-drain charge	Q_{GD}	-	0.7	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.5	-	V	V_{DS} = 400 V; I_D = 3 A

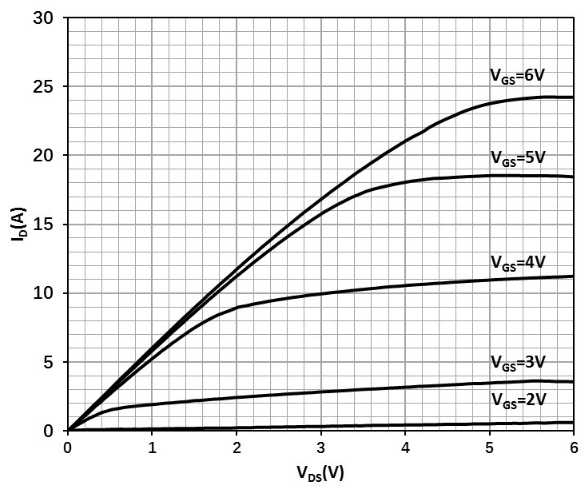
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	V_{GS} = 0 V; I_S = 3 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	18	A	V_{GS} = 6 V; t_{PULSE} = 10 µs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S = 3 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

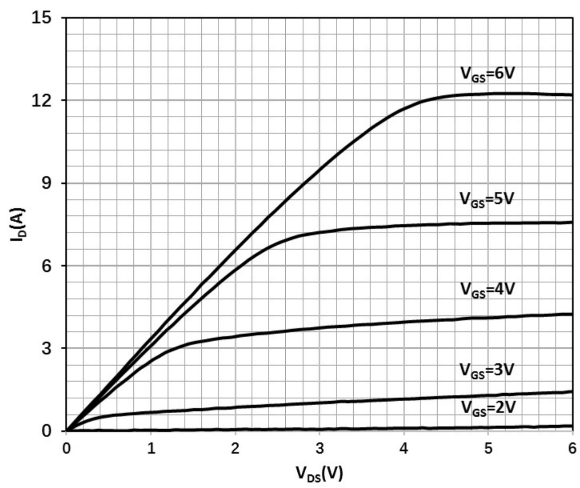
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



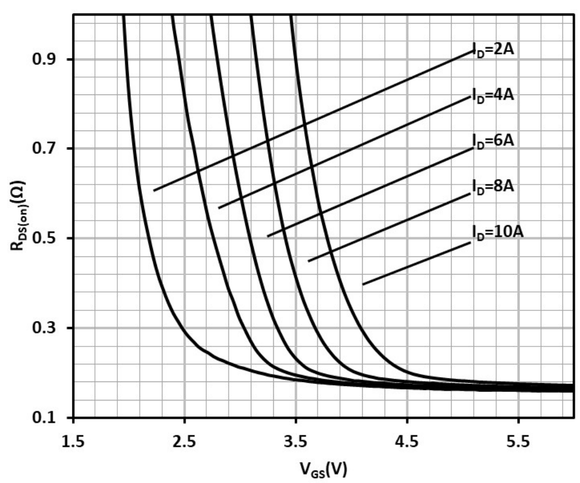
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



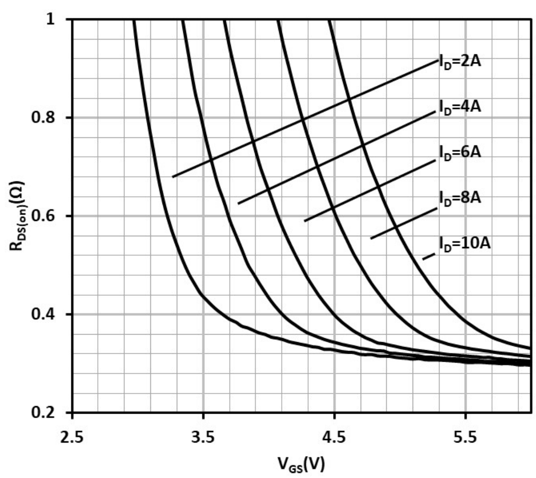
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



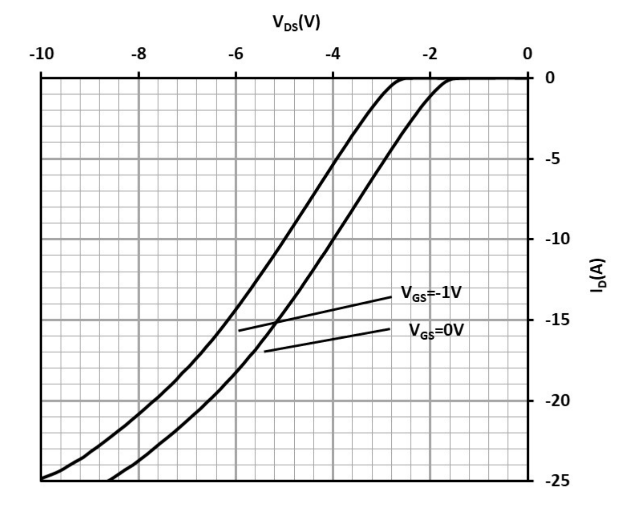
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



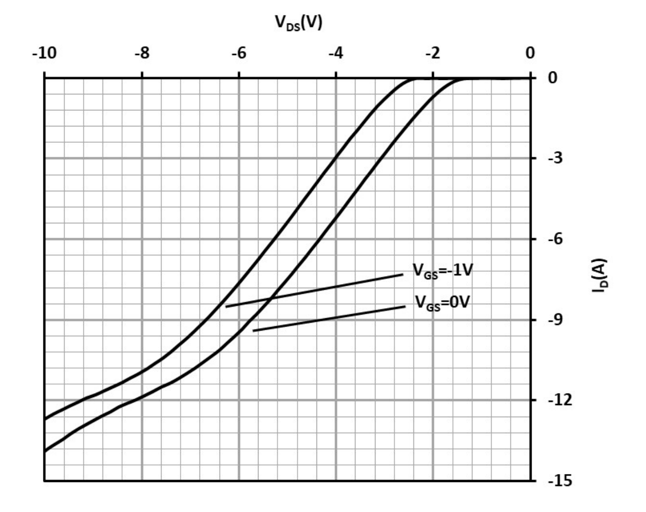
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



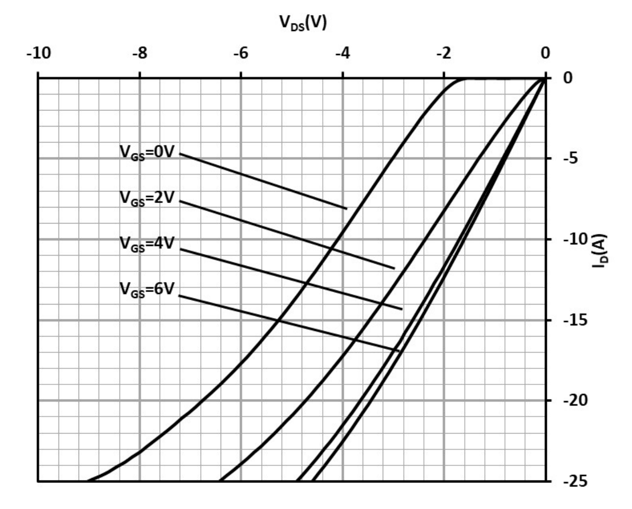
$I_D = f(V_{DS}, V_{GS})$; T_j= 25 °C

Figure 6 Typ. channel reverse characteristics



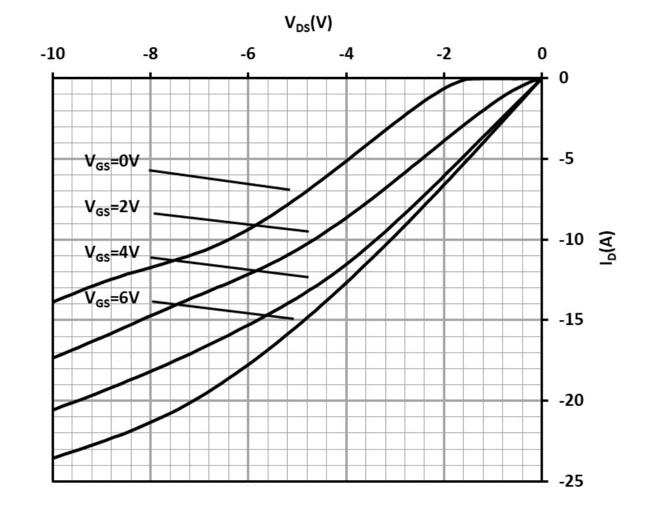
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. channel reverse characteristics



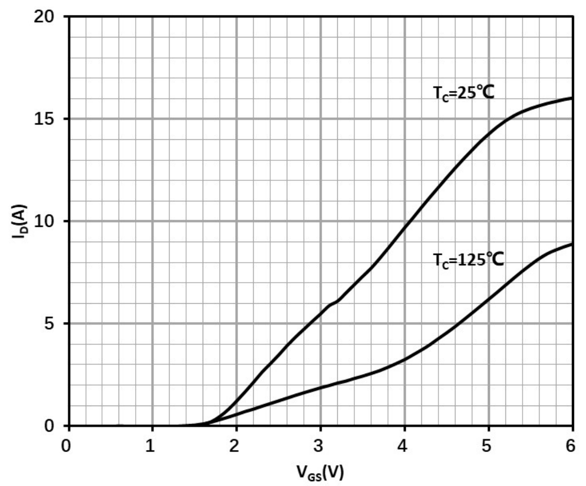
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 8 Typ. channel reverse characteristics



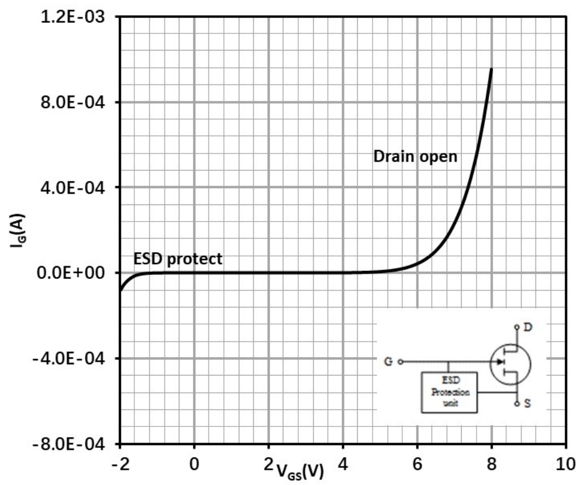
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



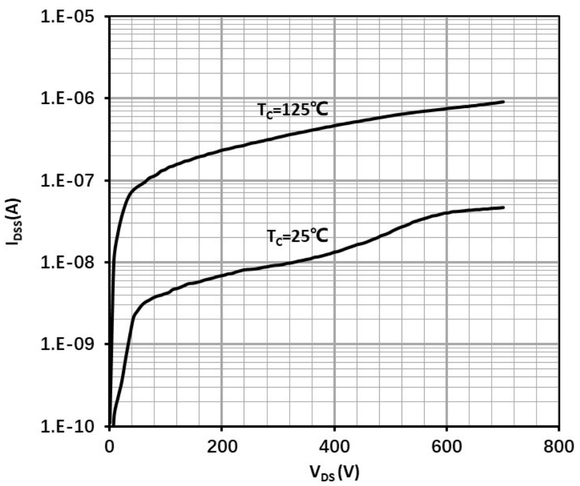
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



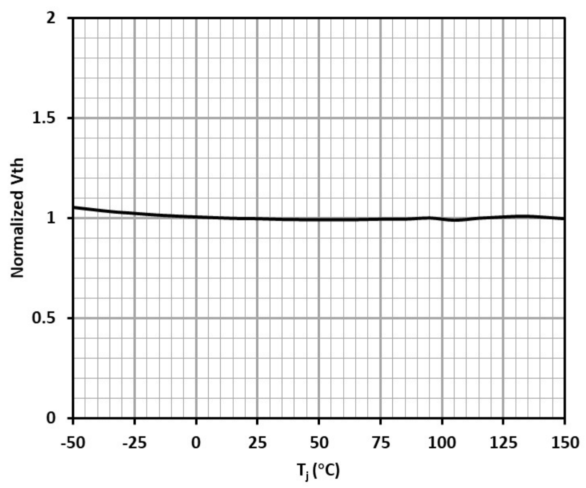
$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



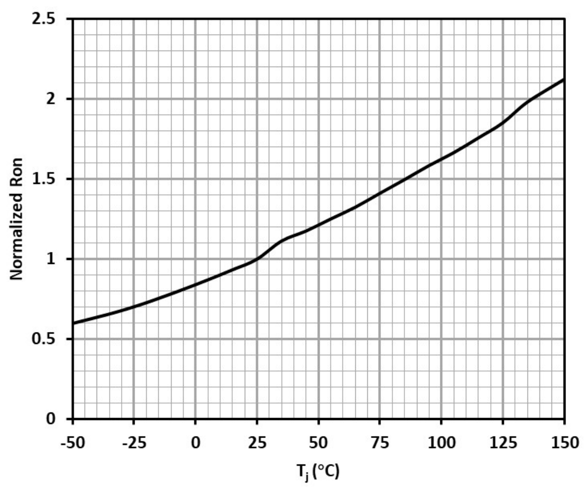
$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



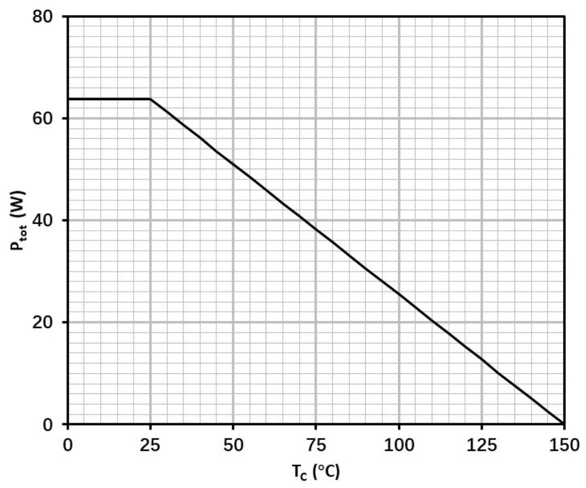
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 11$ mA

Figure 13 Drain-source on-state resistance



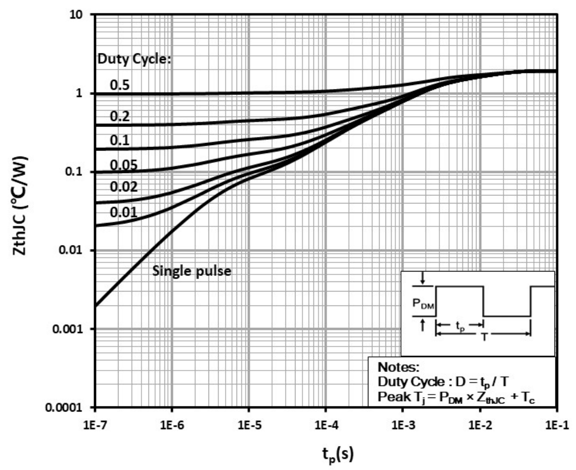
$R_{DS(on)} = f(T_j)$; $I_D = 3$ A; V_{GS}=6V

Figure 14 Power dissipation



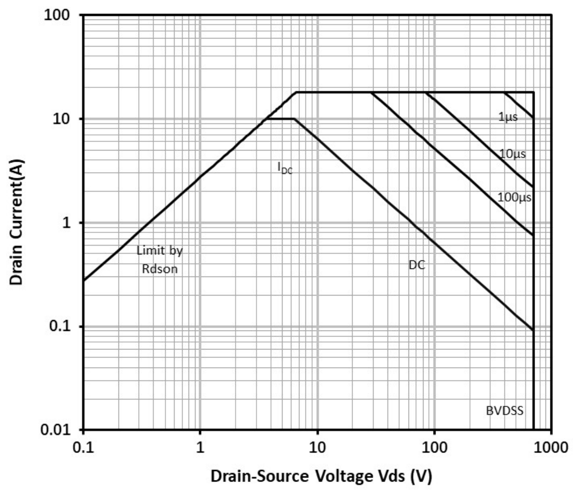
$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



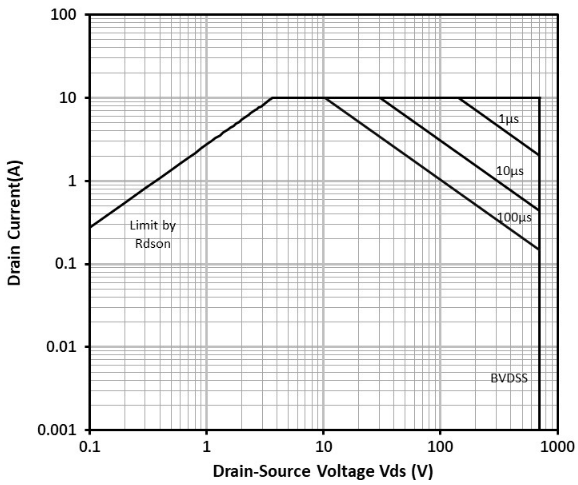
$Z_{thJC} = f(t_P, D)$

Figure 16 Safe operating area



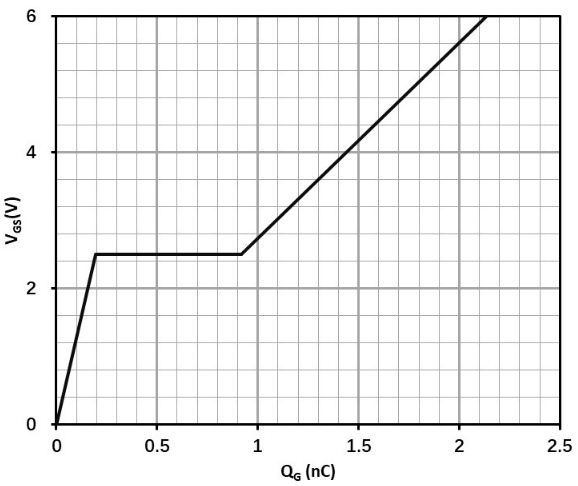
$I_D = f(V_{DS})$; $T_C = 25$ °C

Figure 17 Safe operating area



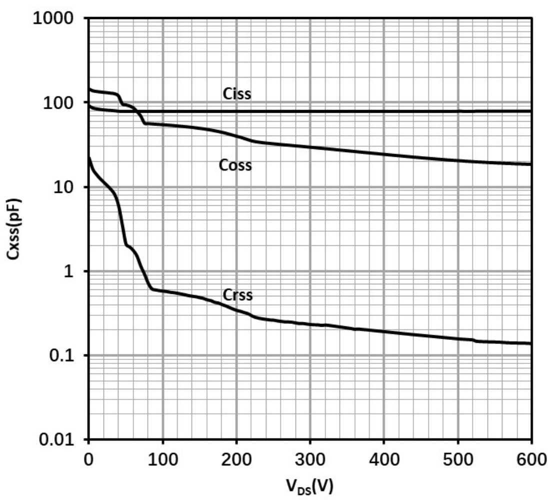
$I_D = f(V_{DS})$; $T_C = 125$ °C

Figure 18 Typ. gate charge



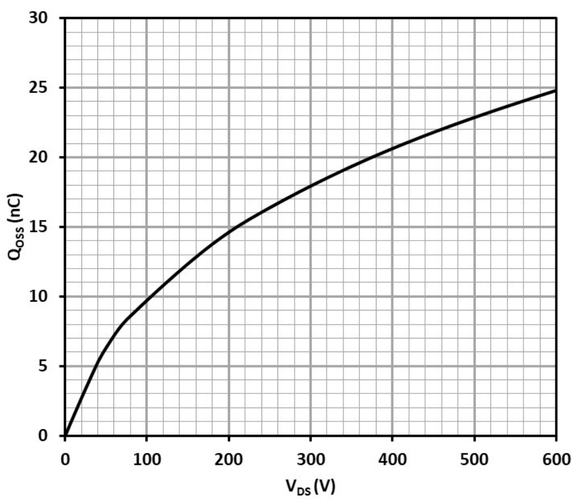
$V_{GS} = f(Q_G)$; $V_{DCLINK} = 400$ V; $I_D = 3$ A

Figure 19 Typ. capacitances



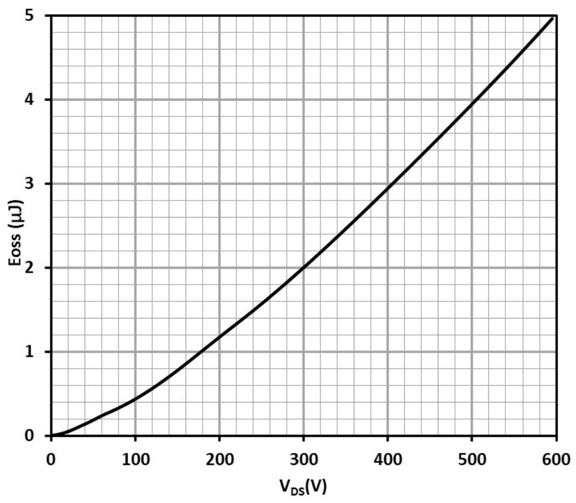
$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 20 Typ. output charge



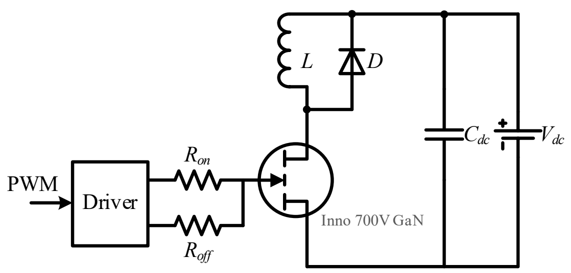
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 21 Typ. C_{OSS} stored Energy



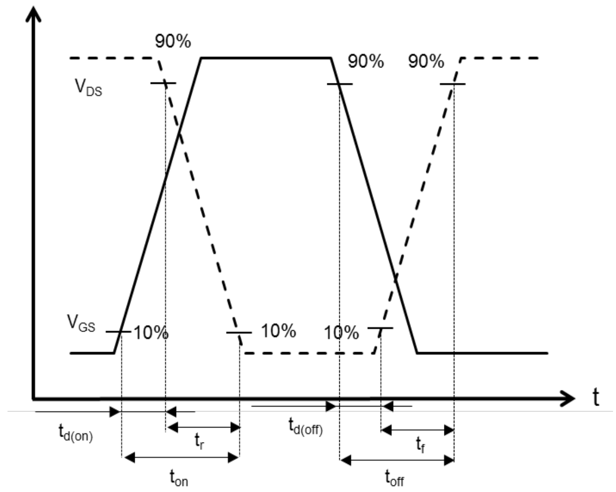
$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load

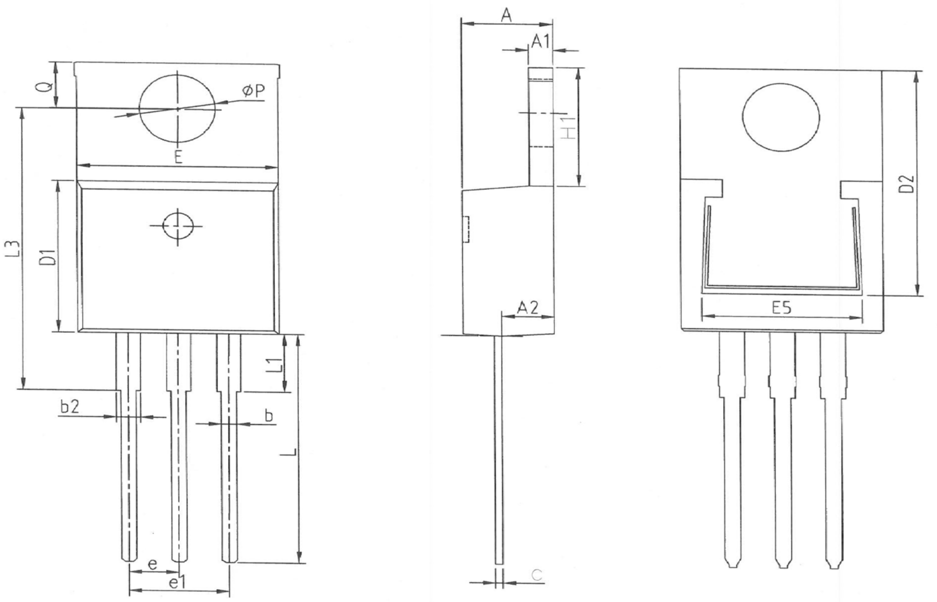


V_{DS} = 400 V, I_D = 6 A, L = 318 µH, V_{GS} = 6 V,
R_{on} = 10 Ω, R_{off} = 2 Ω

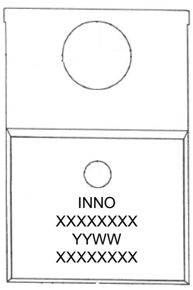
Figure 23 Typ.Switching times waveform



10. Package outlines



SYMBOL	MM			SYMBOL	MM		
	MIN	NOM	MAX		MIN	NOM	MAX
A	4.37	4.57	4.77	E5	6.80	8.20	8.60
A1	1.22	1.27	1.42	e	2.54 BSC		
A2	2.49	2.69	2.89	e1	5.08 BSC		
b	0.75	0.81	0.96	H1	6.10	6.30	6.50
b2	1.22	1.27	1.47	L	13.10	13.40	13.70
c	0.30	0.38	0.48	L1	-	3.75	4.10
D1	8.50	8.70	8.90	L3	15.80	16.00	16.40
D2	12.00	12.40	12.80	ΦP	3.70	3.84	3.99
E	9.86	10.16	10.36	Q	2.54	2.74	2.94



ROW	Description	Example
Row1	Company name	INNO
Row2	Product code	XXXXXXXX
Row3	Date code	YYWW
Row4	ASSY lot No.	XXXXXXXX

Notes:
(1) All dimension are in millimeters.
(2) Drawing is not to scale.
(3) Dimensions do not include mold protrusion.
(4) Package outline exclusive of metal burr dimensions.

11. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-04-21	1.0 version release

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